**Design Review 1**

**Team DIC-sie Chicks**

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To be ready for the first design review, team DIC-sie Chicks first had to create the four schematics of an 8-bit AND gate and an 8-bit OR gate, an 8-bit PASS A connectivity, and a 1-bit 8:1 MUX. To construct the AND and OR gates, a 1-bit, 2-input gate was made of each, and then the created symbol was replicated 8 times and connected together to construct the 8-bit gates. A symbol for the final 8-bit gates was also created. The 8:1 MUX was created using seven 2:1 MUXes. We had concluded that we could create a 8:1 MUX by using two 4:1 MUXes and a 2:1 MUX that combines the two respective outputs. Therefore, we constructed a 2:1 MUX and combined three 2:1 MUXes to create the 4:1 MUX. Given this, we found that an 8:1 MUX is equivalent to seven 2:1 MUXes put together.

The logic gates were then simulated to demonstrate their success. In order to simulate, an 8-bit inverter had to be created so that 2 inverters in series could drive the inputs to the simulated components. A 1-bit inverter was created and then turned into an 8 bit inverter the same way as the AND and OR gates. All logic gates were now ready to be simulated. This was done using ADE L transient simulation. For the AND and OR gates, all four possible input combinations of a 1-bit gate , which are 00, 01, 10, and 11, were tested by checking the transient graphs.

For the second design review, an 8-bit ADD gate, a two’s compliment, and a SHIFT gate will be created in Cadence. Furthermore, the ALU will have in and out connectivity and working registers. All of these additional aspects will be simulated to make sure that they are working properly.

After the second design review, a 4 page final report will be written along with a final PowerPoint presentation. During this design review we also designed a block diagram of the ALU block in Logisim. After this design review has been turned in, we will look more into how to simulate in Ocean and other simulation programs implemented in Cadence such as VHDL. We hope to work on our simulation skills in the next week so that the next part of the project works smoothly and we don’t have issues again. We will also be designing the last components of our ALU so that we can be able to put the project together. We have the NOP, 2Comp, and Arbitrary to do since we don’t have to do the shifter, being a group of three.